1. Introduction

1.1 System Overview

The ROBO-603 is a compact 5.25” CD-ROM size Single Board Computer that equips with VIA Apollo Pro 133A AGPset, SMI AGP 2X Lynx3DM 2D/3D Graphics and Multimedia Accelerator w/ Embedded 4MB SGRAM, Dual LCD interfaces, NTSC/PAL TV output, AC97 Audio, and dual PCI-bus Ethernet interfaces.

Targeting on the rapid growing networking and multimedia embedded markets, the ROBO-603 comes designed with dual PCI-bus Intel 82559ER 10/100Base-Tx chips and dual LCD interfaces. This make it a perfect solution for not only popular Networking Devices like Firewall, Gateway, Router, Thin Server, and E-Box but also Retail / Financial Transaction Terminals, and high-end multimedia POS / KIOSK Terminals.

In addition, the on board 24-bit Panel Link interface, Zoom Video port, and NTSC/PAL TV output interface make the ROBO-603 also ideal for demanding high-end Entertainment Devices that require high integration multimedia Single Board Computer.

Other impressive features include PC133 FSB, Ultra DMA66 IDE, a Compact Flash socket for type I/II Compact Flash storage card, four serial ports, one parallel port, one 168-pin DIMM socket allowing for up to 256MB of SDRAM to be installed, and a PCI slot for future expansion.

1.2 Check List

- 1 ROBO-603 All-in-One FC370 Celeron / Pentium III Computing Module
- 1 Quick Installation Guide
- 1 CD-ROM contains the followings:
  - — User’s Manual (this manual in PDF file)
  - — Ethernet driver and utilities
  - — VGA drivers and utilities
  - — Audio drivers and utilities

Latest BIOS (as of the CD-ROM was made)

1.3 System Specifications

General Functions

- **CPU:** Intel FC-370 Pentium III/Celeron (with system bus frequencies of 66/100/133MHz)
- **CPU socket:** Intel Socket 370
- **BIOS:** Award 256KB Flash BIOS
- **Chipset:** VIA Apollo Pro 133A, VT82C694X
- **I/O Chipset:** VT82C686A / Winbond W83977EF-AW
- **Memory:** Onboard one 168-pin DIMM socket supports up to 256 Mbytes SDRAM
- **Enhanced IDE:** Supports two IDE devices. Supports Ultra DMA/66 mode with data transfer rate up to 66MB/sec. (20 x 2 header onboard)
- **FDD interface:** Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB and 2.88MB)
- **Parallel port:** One bi-directional parallel port. Supports SPP, ECP, and EPP modes
- **Serial port:** Three RS-232 and one RS-232/422/485 serial port. Ports can be configured as COM1, COM2, COM3, COM4, or disabled individually. (16C550 equivalent)
- **IR interface:** Supports one IrDA Tx/Rx header
- **KB/Mouse connector:** 8-pin (4 x 2) connector supports PS/2 keyboard and mouse
- **USB connectors:** One 5 x 2 header onboard supports dual USB ports
- **Watchdog Timer:** Can generate a system reset, IRQ15 or NMI. Software selectable time out interval (32 sec. ~ 254 min., 1 min./step)
- **DMA:** 7 DMA channels (8237 equivalent)
- **Interrupt:** 15 interrupt levels (8259 equivalent)

- **Power management:** Supports ATX power supply. Supports PC97, LAN wake up and modem ring-in functions. I/O peripheral devices support power saving and doze/standby/suspend modes. APM 1.2 compliant.

Flat Panel/CRT Interface

- **Chipset:** SMI Lynx3DM SM721, high performance 128-bit GUI, 3D engine
- **Display memory:** 4 MB of SGRAM frame buffer on Lynx3DM SM721G4. Optional 8 MB SGRAM frame buffer on Lynx3DM SM721G8
- **Display type:** Simultaneously supports CRT and flat panel (EL, LCD and gas plasma) displays
- **Interface:** 2X AGP, Accelerator Graphics Ports 1.0 compliant
- **Display mode:**

  LCD panel supports up to 800 x 600 @ 24 bpp, 1024 x 768 @ 24 bpp

  CRT displays support up to 800 x 600 @ 24 bpp, 1024 x 768 @ 24 bpp
- **Video capture port:** 40-pin YUV Direct Video Input Port onboard
- **TV output interface:** Supports both RCA jack and S terminal

Panel Link (Optional)

- **Chipset:** Sil 164 PanelLink Digital Transmitter
- **Scalable bandwidth:** Ranging from 25 ~ 112 MHz (VGA ~ SXGA); 24/48-bit one/two pixel per clock

Audio Interface

- **Chipset:** VT82C686A
- **Audio controller:** AC97 ver. 2.0 compliant interface, Multi-stream Direct Sound and Direct Sound 3D acceleration
- **Audio interface:** Microphone in, Line in, CD audio in, line out, Speaker L, Speaker R

Ethernet Interface

- **Chipset:** Dual Intel 82559ER PCI-bus Ethernet controllers onboard
- **Ethernet interface:** PCI 100/10 Mbps, IEEE 802.3U compatible
- **Remote Boot-ROM:** For diskless system

SSD Interface

One CF socket supports Type I/II Compact Flash Card

Expansion Interface

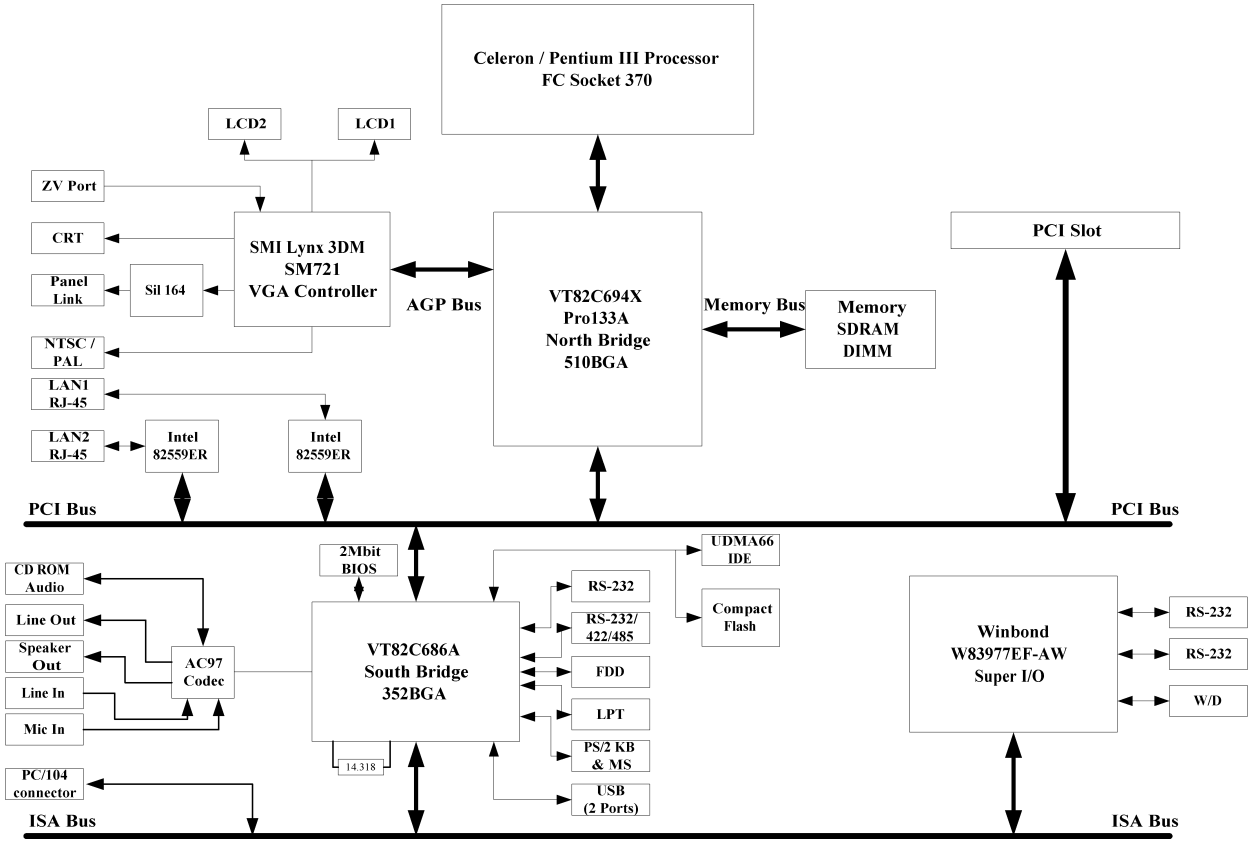
- **PC/104 connector:** One 16-bit 104-pin connector onboard
- **PCI slot:** One 32-bit PCI slot onboard

Mechanical and Environmental

- **Power supply voltage:** ATX type, +5V and +12V
- **Typical power requirement:** 5V @ 5.2A, 12V @ 80mA w/ PIII 800MHz & 128MB SDRAM
- **Operating temperature:** 32 to 140°F (0 to 60°C)
- **Board size:** 8”(L) x 5.75”(W) (203mm x 146mm)
- **Weight:** 0.5 Kg

1.4 Architecture Overview

The following block diagram shows the architecture and main components of ROBO-603.



The two key components on board are the VIA VT82C694X North Bridge and VT82C686A super South Bridge. These two devices provide the ISA and PCI bus to which all the major components are attached.

The following sections provide detail information about the functions provided onboard.

1.4.1 VIA VT82C694X

The VIA VT82C694X along with the VT82C686A companion chip provide the basic functionality and buses of the system:

- High Performance CPU interface.
- Full Featured Accelerated Graphics Port (AGP) controller.
- Advanced High-Performance DRAM controller. PC133 compliant SDRAM must be used if 133MHz FSB CPU is to be used.
- Concurrent PCI Bus controller.
- PCI to ISA Bridge provided by VT82C686A super south bridge.
- Universal Serial Bus controller integrated in the VT82C686A.

- UltraDMA-33 / 66 Master Mode PCI EIDE controller. Two connectors are provided: A 40 pin pitch 2.54mm standard IDE interface on the primary controller and a Compact Flash connector on the secondary controller.
- SoundBlaster Pro hardware and Direct Sound ready AC97 Digital Audio controller.

1.4.2 DRAM Interface

The VT82C694X supports eight banks of DRAMs up to 1.5GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM controller can run at either the host CPU bus frequency (66 /100 /133MHz) or at the AGP bus frequency (66 MHz) with built-in PLL timing control.

1.4.3 AGP Interface

The VT82C694X system controller also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

1.4.4 PCI Interface

The VT82C694X supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

1.4.5 VIA VT82C686A

The VT82C686A PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686A includes standard intelligent peripheral controllers:

- Two 16550-compatible serial I/O ports with infrared communications port option on the second port.
- LPT. Support for SPP, EPP and ECP modes.
- Standard floppy disk drive interface.
- Keyboard controller with PS2 mouse support.
- Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.
- Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.
- Full System Management Bus (SMBus) interface.

- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.
- Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.
- Internal I/O APIC (Advanced Programmable Interrupt Controller).

1.4.6 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C686A also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The VT82C686A also supports the UltraDMA-66 standard. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

Access to these controllers is provided by one standard IDC 40-pin connector and one Compact Flash type II connector.

1.4.7 USB

The Universal Serial Bus controller is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686A includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

1.4.8 SMI Lynx3DM SM721 VGA Controller

The Lynx3DM consists of a logic block, which interfaces to a 4MB or 8MB block of integrated memory. The integrated memory supports single clock cycle transfers up to 100MHz. Peak memory bandwidth for the integrated 128-bit memory bus is over 1.6GB/s.

The logic within the Lynx3DM consists of 11 functional blocks: PCI Interface, Host Interface (HIF), Memory Controller, Drawing Engine, Power Down Control Unit, Video Processor, Video Capture Module, LCD Backend Controller, VGA Core, PLL Module, and RAMDAC. A summary of each of the functional blocks, along with important features follows:

- AGP 2X sideband support
- PCI 2.1 compliant
- 33 MHz PCI Master/Slave interface
- Dual aperture feature for concurrent VGA and video/drawing engine access

- Independent memory interface control
- Up to 128-bit memory interface
- Over 1.6GB/s memory bandwidth
- 100MHz single clock/cycle engine
- Designed to accelerate DirectDraw and Direct3D
- IEEE Floating Point Setup Engine
- Complete 3D Rendering Engine set:
  - Bi-linear and tri-linear filtering
  - Mip Mapping
  - Vertex and global fog
  - Source and destination alpha blend
  - Specular highlights
  - Edge anti-aliasing
  - Z-buffering
  - Gouraud shading
  - Mirrored textures
  -Texture decompression
- Offloads motion compensation portion of MPEG-2 decode process from CPU

- Separate bus master control for motion compensation command and IDCT data
- Sub-picture support
  - 2-bit/pixel format
  - 8-bit/pixel format
- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Macrovision function (version 7.1.21)
- Closed captioning function
- Dynamic Power Management
- Virtual Refresh
- Standby and Suspend model support
- ACPI, DPMS, APM compliant
- Multiple video windows in HW
- Independent video sources on different displays
- Bi-linear scaling
- Flicker filter and underscan for TV display
- Support for Zoom Video Port interface
- Crop, filter, shrink support
- TFT and DSTN support up to SXGA
- Timing generation for Virtual Refresh
- Popup icon location flexible
- Transparency color support
- 100% IBM VGA compatible
- Separate PLL for LCD panel timing
- 200MHz speed provides resolution support to 1600x1200.

1.4.9 Panel Interface

An alternative display to the standard CRT monitor is digital flat panel interfaces in which the color of each pixel is digitally encoded. The panel data may be transferred in parallel where the color of each pixel is transferred over a number of signal lines at rates up to 80MHz.

Lynx3DM supports both color dual scan STN (passive) and color TFT (active) panel interface. It can also support color TFT panel with RGB analog interface. For color DSTN panel, Lynx3DM can support 16-bit and 24-bit interfaces up to 1600x1200 resolution. For color TFT panel, Lynx3DM can support single pixel per clock of 9-bit, 12-bit, 18-bit, 24-bit, or double-pixel per clock of 24-bit, 36-bit interfaces up to 1280x1024 resolution.

Lynx3DM supports two separate digital LCDs. Both LCDs need to be TFT interface. FP1 has to be only 18-bit TFT interface and FP2 has to be 24-bit TFT interface. DSTN panel can not be supported under dual digital LCD mode. Dual Digital LCD mode is supported through the Virtual Refresh architecture. FP1 and FP2 must be in Virtual Refresh mode. FP1 clocks the data based on VRCLK (Virtual Refresh Clock); whereas FP2 clocks the data based on FIFOCLK (based on Video Clock).

The parallel interface is only suitable for short distance (less than 50 cm) and is typically implemented by using of ribbon cables. One should be careful in the EMC design of the box and cabling when this interface is used.

It should also be noted that the signal level of this interface is 3.3V, but does comply with the TTL signal levels. Some - most older displays require 5V signal level.

1.4.10 Zoom Video Port

Lynx3DM's Zoom Video Port (ZV Port) is designed to interface with video solutions implemented as PCMCIA (or PC CardBus) cards: examples are NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codecs. The ZV Port can also directly interface with an NTSC/PAL decoder, such as Philips 7111 or BT819.

Incoming video data from the ZV Port interface can be YUV or RGB format. The data can be interlaced or non-interlaced. The ZV Port can be configured for output if the video capture function is disabled. 18-bit graphics and video data in RGB format can be sent out when the ZV Port is configured for output mode. The ZV Port may also be configured as a test port. Up to 20 signals from each of the logic blocks within Lynx3DM can be brought out to an internal test bus (TD Bus) connected to the ZV Port. System designers or silicon validation engineers can access these signals by setting the TEST0, TEST1, USR0, USR1, and USR2 pins. This approach can bring out a total of 180 internal signals to the primary I/O pins. The test port capability can be used to enhance fault coverage, as well as reduces silicon validation or debugging time.

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer.

The Video Capture Unit support several features to maintain display quality, and balance the capture rate:

- 2-tap, 3-tap, and 4-tap horizontal filtering
- 2 to 1 and 4 to 1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swap, RGB 5:5:5, and RGB 5:6:5
- Multiple frame skipping methods
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

Lynx3DM uses the Video Processor block to display the captured data on the LCD, TV, or CRT display. The captured data can be displayed through Video Window I or Video Window II. The stretching, color interpolation, YUV-to-RGB conversion, and color key functions are performed in the Video Processor. Lynx3DM's Video Processor can simultaneously process captured video data and perform CD-ROM playback on two independent video windows.

Lynx3DM also supports real-time video capture to the hard drive or system memory through PCI master mode or slave mode. In PCI bus master mode, Lynx3DM uses the Drawing Engine's Host BLT and Host DMA functions to maximize performance.

1.4.11 TV Encoder

The TV Encoder is an NTSC/PAL Composite Video/S-video Encoder. It receives RGB inputs and converts to digital video signals based on CCIR 624 format.

The input video signal of the TV Encoder is RGB 8-bit each. The sampling rate is corresponding to CCIR 601, Square pixel and 4Fsc (NTSC only).

The output video signals of the TV Encoder are Composite video signal and S-video signals of 10-bit each. These output signals are over-sampled by a double frequency clock called CLKX2. This feature helps to simplify external analog filtering.

The TV Encoder video timing is controlled by vertical sync and the horizontal sync input signals. The blank signal input is optional. If the blank signal input signal is pulled up, internal blanking control will be performed.

Macrovision 7.01 and closed captioning functions are included.

Key features are summarized as the following:

- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Slave timing operation
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Selectable pedestal level OIRE/7.5IRE for NTSC
- Macrovision function (version 7.01)
- Closed aptioning unction

1.4.12 Ethernet

The Ethernet interfaces are based on two Intel 82559ER Ethernet controllers, which support both 100Mbit as well as l0Mbit Base-T interface.

The Ethernet controllers are attached to the PCI bus and use PCI bus mastering for data transfer. The CPU is thereby not loaded during the actual data transfer.

The 82559ER is part of Intel's second generation family of fully integrated 10BASE-T / 100BASE-TX LAN solutions. The 82559ER consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. 82559 family members build on the basic functionality of the 82558 and contain power management enhancements.

The 82559ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82559ER to perform high-speed data transfers over the PCI bus. The 82559ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns, allowing the 82559ER to transmit data with minimum interframe spacing (IFS).

The 82559ER can operate in either full duplex or half duplex mode. In full duplex mode the 82559ER adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The 82559ER includes a simple PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex, and flow control. These features and others reduce cost, real estate, and design complexity.

The 82559ER also includes an interface to a serial (4-pin) EEPROM and a parallel interface to a 128 Kbyte Flash memory. The EEPROM provides power-on initialization for hardware and software configuration parameters

1.4.13 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

1.4.14 Panel Link Interface (Optional)

The SiI164 transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface. The SiI164 transmitter has a highly flexible interface with either a 12-bit mode (½ pixel per clock edge) or 24-bit mode 1-pixel/clock input for true color (16.7 million) support. In 24-bit mode, the SiI164 supports single or dual edge clocking. In 12-bit mode, the SiI164 supports dual edge single clocking or single edge dual clocking. The SiI164 can be programmed though an I2C interface. The SiI164 support Receiver and Hot Plug Detection.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.